MEVD- 101 Digital Signal Processing

Unit I

Review of Discrete time signals: sequences, representation. Discrete time systems: linear, time in variant, LTI systems, properties, and constant coefficients difference equations. Frequency Domain representation of discrete time signals and systems

Unit II

Review of Z Transform – Properties, ROC, Stability, Causality, Criterion. Inverse Z Transform, Recursive and Non Recursive systems, Realization of discrete time system

Unit III

DFT: Properties, Linear and Circular convolution, Discrete Cosine Transform, Relationship between DFT and DCT. Computation of DFT: FFT/Decimation in Time and Decimation in Frequency

Unit IV

FIR and IIR systems: Basic structure of FIR and IIR, Bilinear Transformation, Design of Discrete time IIR filter-Butterworth, Chebychev, Inverse Chebychev, Elliptic etc. Design of FIR filters by windowing – Rectangular, Bartlett, Hann, Hamming, Kaiser, Window filter, Design method relationship of Kaiser to other window. Application of MATLAB for Design of Digital filter. Effect of Finite register length in filter Design

Unit V

Discrete time Random signals: Discrete time random process, Averages, Spectrum Representation of finite energy signals, response of linear systems to random signals. Power spectrum estimation: Basic principles of spectrum estimation, estimate of auto con variance, power spectrum ,cross con variance and cross spectrum. Advance signal processing technique and transforms: multi rate signal processing- down sampling/up sampling, introduction to discrete Hilberts Transform, Wavelet Transform, Haar Transform etc.

Text/References:

1. Discrete time signal processing by Opperenheim & Schaffer PHI.
2. Digital Signal Processing using MATLAB by S.Mitra
3 Digital Signal Processing By Proakis Pearson Education
4. Theory & application of Digital Signal Processing by L.R.Rabiner & B. Gold PHI

MEVD 102 CMOS VLSI Design

Unit I

VLSI design methodologies: VLSI Design flow, Design Hierarchy, Regularity, Modularity and Locality, VLSI design styles, Introduction to MOSFETs: MOS Inverter, Static and Switching Characteristics, Voltage Transfer characteristics, Noise Margin, Issues of Scaling. Second order effects, the complementary CMOS, Inverter DC characteristics.

Unit II

Static Characteristics of Resistive Load Inverter, Inverters with n-Type MOSFET Load , CMOS Inverter ,Introduction of Switching Characteristics , Delay Time , Determination of delay Times , Inverter Design with Delay Constraints , Estimation of Interconnect Parasitics , Calculation of Interconnect Delay , power Dissipation of CMOS inverters.

Unit III

CMOS Process Enhancement and Layout Considerations: Interconnect, circuit elements, Stick diagram, Layout design rules, Latchup, latchup triggering, latchup prevention, Technology related CAD issues.

Unit IV

Subsystem Design: Structured design of combinational logic- parity generator, Multiplexer, code converters. Clocked sequential circuits, two phase clocking, charge storage, dynamic register element, dynamic shift register. Subsystem design process, Design of ALU subsystem, Adders, Multipliers. Commonly used storage/ memory elements.

Unit V

Field Programmable Devices: Definitions of Relevant Terminology, Evolution of Programmable Logic Devices, User- Programmable Switch Technologies, Computer Aided Design (CAD) Flow for FPDs, Programmable Logic, Programmable Logic Structures, Programmable Interconnect, Reprogrammable Gate Array, Commercially Available SPLDs, CPLDs and FPGAs, Gate Array Design, Sea-of-Gates.

Text/ References Books:

1. Neil H.E. Weste and Kamran Eshraghian, “Principles of CMOS VLSI Design - A System Perspective”, Pearson Education ASIA.

2. John P. Uyemura, “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc.,

3. D.A. Pucknell, K. Eshraghian, Basic VLSI Design, PHI.

4. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons.

5. Mead and L. Conway, Introduction to VLSI Systems, Addison-Wesley.

6. A. Mukherjee, Introduction to nMOS and CMOS VLSI systems design, Prentice Hall.

MEVD 103 (A) Advanced Logic Design

UNIT I

SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Structure and Operation of Clocked Synchronous Sequential Networks, Analysis of Clocked Synchronous

Sequential Circuits: Modeling of Clocked Synchronous Sequential Network Behavior, Serial Binary Adder

Using Mealy and Moore Networks: Sequence Recognizer, State Table Reduction, State Assignment, Design of Clocked Synchronous Sequential Circuits.

UNIT II

SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN USING ASM Algorithmic State Machine, ASM Charts, ASM Blocks ,Sequence Recognition Using ASM Charts, State Assignments, ASM Transition Tables, ASM Excitation Tables ,ASM Realization Using Discrete Gates , Multiplexers ,Design of Iterative Circuits.

UNIT III

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN Structure and Operation of Asynchronous Sequential Networks, Analysis of Asynchronous Sequential Circuit, Races and Hazards in Asynchronous Sequential Networks, Primitive Flow Table, Reduction of Input Restricted Flow Tables, Flow Table Reduction, State Assignment Problem and the Transition Table, Design of Asynchronous Sequential Circuits.

UNIT IV

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES: Programming logic device families, PLAs, PROMs ,Designing a synchronous sequential circuit using PLA/PAL ,Realization of finite state machine using PLD , FPGA ,Xilinx, FPGA-Xilinx 4000.

UNIT V

SYSTEM DESIGN USING VERILOG: Hardware Modelling with Verilog HDL, Logic System, Data Types and Operators For Modelling in Verilog HDL , Behavioral Descriptions in Verilog HDL, HDL Based Synthesis, Synthesis of Finite State Machines, structural modeling , compilation and simulation of Verilog code ,Test bench , Realization of combinational and sequential circuits using

Verilog , Registers, counters ,sequential machine ,serial adder ,Multiplier, Divider ,Design of simple microprocessor.

Text/ Reference Books:

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill, .

2. William I. Fletcher, “An Engineering Approach to Digital Design”, Prentice Hall India.

3. Charles H. Roth Jr,“Fundamentals of Logic design”, Thomson Learning.

4. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India.

1. John F. Wakerly, Digital Design, Pearson Education Asia.

2. M. M. Mano, Digital Design, Pearson Education .

3. C. H. Roth, Jr., Fundamentals of Logic Design, Jaico Publishing House.

4. Fletcher, An Engineering Approach to Digital Design, PHI.

5. J. M. Yarbrough, Digital Logic, Thomson Learning.

6. Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, McGraw-Hill Higher Education.

7. Samir Palnitkar, Verilog HDL, Prentice Hall.

MEVD 103 (B) VLSI SIGNAL PROCESSING

UNIT I

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT II

Pipeline interleaving in digital filters. Pipelining and parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters, Combining Pipelining and Parallel Processing

UNIT III

Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

UNIT IV

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

UNIT V

Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Text/ Reference Books:

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences.

2. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing,

McGraw Hill.

3. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singal processing, Prentice Hall.

4. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall.

MEVD – 104 (A) Embedded Microcontrollers Programming

Unit-I

Embedded System Overview : Embedded System definition. Processor Technology, General purpose, Single Purpose, Application Specific, Super scalar, Pipelined, Very Long Instruction Word (VLIW) Processor, Microprocessors, Micro controllers and DSP Processors. Embedded Processors in VLSI circuit.

Unit-II

Architectural Issues : CISC, RISC, DSP and Harvard/Princeton Architectures. Memory : ROM, EPROM, EEPROM, FLASH, RAM, SRAM, DRAM, SDRAM, NVRAM, EDORAM, DDRRAM, Memory Hierarchy and Cache. Interfacing : Interfacing using Glue Logic, Interrupt, DMA, I/O Bus structure, I/O devices, Serial Communication Protocols, Parallel Communication Protocols, Wireless Protocols.

Unit-III

Introduction to 8-bit Microcontrollers e.g. 8051, 68HC11, 80196, Timers/Counters, USART. Detailed study of 8051 microcontroller, with its programming in assembly language and Interrupts, Serial Programming etc.

Unit-IV

Interfacing of Microcontroller such as SPI, PWM, WDT, Input Capture , Output Compare Modes, Interfacing LED, Switches, ADC, DAC, LCD , RTC. Idea about the C programming of Microcontroller. I2C, CAN bus architecture.

Unit-V

Introduction to 16/32-bit microcontrollers. Introduction to ARM Architecture and Organization, Difference between ARM7 , ARM9 & ARM11 TDMI, ARM programming model, ARM Instruction set.

Text/References Books:

1. David E. Simon, An Embedded Software Primer, Pearson Education.
2. Dr. RajKamal, Embedded Systems, TMH.

3. Vahid & Givargis, Embedded System Design,John Wiley & Sons.

4. K. J. Ayala , 8051 Microcontrollers, Penram International.

5. M. A. Mazidi & J. G. Mazidi, 8051 Microcontroller and Embedded System, Pearson Education Asia

6. J. W. Valvano, Embedded Microcomputer Systems - Real Time Interfacing, Thomson Asia Pte. Ltd.

7. R. H. Barnett, 8051 family of Microcontrollers, PHI.

8. Peter Spasov, Microcontroller Technology: The 68HC11, PHI.

9. Dr. Rajkamal, Microcontrollers (Architecture, Programming, Interfacing and System Design), Pearson Education.

MEVD – 104 (B) SOLID STATE DEVICES

Unit-I

PHYSICS OF SEMICONDUCTOR AND PN JUNCTION

Allowed and Forbidden Bands, Band Structure, Density of States Function, Statistical Mechanics, Electrical Conduction Semiconductor In Equilibrium, Carrier Transport Phenomena, Non-Equilibrium Excess Carries in Semiconductor, PN Junction Current, Small Signal Model, Generation And Recombination Current, Junction Break Down

Unit-II

MOS CAPACITOR and MOSFET:

Metal Semiconductor and Hetero Junctions, Two Terminal MOS Structure, CV Characteristics, MOSFET Operation, I-V derivation, Frequency Limitation, Short channel effects, MOSFET scaling, Radiation, and hot electron effect

Unit-III

LARGE SIGNAL AND LOW-FREQUENCY SMALL SIGNAL MODELING :

Quasi-Static modeling and Non quasi static modeling of MOSFET, Transit time, Equivalent model of MOSFET with extrinsic resistance and capacitance, low frequency small signal modeling for weak, moderate and strong region of operation.

Unit-IV

Advanced MOSFETs :Strain Engineered Channel materials, Mobility in strained materials, Electrostatics of double gate, and Fin-FET devices SOI MOSFET: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT definitions, Back gate coupling and body effect parameter, I-V characteristics of FDSOI-FET, FDSOI-sub-threshold slope, Floating body effect, single transistor latch, ZRAM device,

Unit-V

ADVANCE MOS DEVICES: High Electron Mobility Transistor (HEMT): physical structure of HEMT, quantum well structures, 2D electron gas density, charge voltage relation, current voltage characteristics, cut-off frequency

Text/References Books:

1. S. M. Sze, “Semiconductor Devices, Physics And Technology”, John Wiley and Sons.
2. K. Hess, Advanced Theory of Semiconductor Devices, Prentice-Hall
3. Yannis Tsividis, Operation and Modelling of the MOS Transistor, Oxford University Press
4. J.P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Springer
5. Michael Shur, Physics of Semiconductor Devices, Prentice Hall
6. Donald Neaman, “Semiconductor Physics and Devices”, McGraw Hill, 4 th Edition, 2012
7. S. M. Sze, “Physics of Semiconductor Devices”, John Willey 3 rd Edition, 2007
8. B. G. Streetman,“Solid State Electronics Device”, HI, 2005
9. Y. Tsividis, Colin McAndrew, “Operation And Modeling Of The MOS Transistor”, Oxford university press,
11. Y. Taur and H. Ning, “Fundamentals of Modern VLSI Devices” Cambridge University Press,

MEVD 105 RESEARCH METHODOLOGY AND IPR

UNIT 1

INTRODUCTION TO RESEARCH METHODS

Definition and Objective of Research, Various steps in Scientific Research, Types of Research, Criteria for Good Research, Defining Research Problem, Research Design , Case Study Collection of Primary and Secondary Data, Collection Methods: Observation, Interview, Questionnaires, Schedules,

UNIT 2

SAMPLING DESIGN AND HYPOTHESIS TESTING

steps in Sampling Design, Types of Sample Designs, Measurements and Scaling Techniques - Testing of hypotheses concerning means (one mean and difference between two means -one tailed and two tailed tests), concerning variance – one tailed Chi-square test.

UNIT 3

INTERPRETATION AND REPORT WRITING

Techniques of Interpretation, Precaution in Interpretation, Layout of Research Report, Types of Reports, Oral Presentation, Mechanics of Writing Research Report

UNIT 4

INTRODUCTION TO INTELLECTUAL PROPERTY

Introduction, types of intellectual property, international organizations, agencies and treaties, importance of intellectual property rights, Innovations and Inventions trade related intellectual property rights.

UNIT 5

TRADE MARKS, COPY RIGHTS AND PATENTS

Purpose and function of trade marks, acquisition of trade mark rights, trade mark registration processes, trademark claims –trademark Litigations- International trademark law

Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.

Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer

Text/References Books:

1. C.R. Kothari, Gaurav Garg, Research Methodology Methods and Techniques, New Age International Publishers.

2. Deborah E. Bouchoux, “Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets”, Delmar Cengage Learning.

3. Prabuddha Ganguli, “Intellectual Property Rights: Unleashing the Knowledge Economy”, Tata McGraw Hill Education.

4. Panneerselvam, R., Research Methodology, Prentice-Hall of India, New Delhi,.

5. Ranjith Kumar, Research Methodology – A step by step Guide for Begineers, Sage publisher.

6. D Llewelyn & T Aplin W Cornish, “Intellectual Property: Patents, Copyright, Trade Marks and Allied Rights”, Sweet and Maxwell, .

7. Ananth Padmanabhan, “Intellectual Property Rights-Infringement and Remedies”, Lexis Nexis,

8. Ramakrishna B and Anil Kumar H.S, “Fundamentals of Intellectual Property Rights: For Students,Industrialist and Patent Lawyers”, Notion Press.

9. M.Ashok Kumar and Mohd.Iqbal Ali :”Intellectual Property Rights” Serials Pub.

MEVD-106 LAB I Digital Signal Processing

List of Experiments:

1. Generate the following standard discrete time signals. i) Unit Impulse ii) Unit step iii) Ramp iv) Exponential v) Sawtooth

2. Generate sum of two sinusoidal signals and find the frequency response (magnitude and phase).

3. Implement and verify linear and circular convolution between two given signals.

4. Implement and verify autocorrelation for the given sequence and cross correlation between two given signals.

5. Compute and implement the N-point DFT of a given sequence and compute the power density spectrum of the sequence.

6. Implement and verify N-point DIT-FFT of a given sequence and find the frequency response (magnitude and phase).

7. Implement and verify N-point IFFT of a given sequence.

8. Design IIR Butterworth filter and compare their performances with different orders (Low Pass Filter /High Pass Filter)

9. Design IIR Chebyshev filter and compare their performances with different orders (Low Pass Filter /High Pass Filter).

10. Design FIR filter (Low Pass Filter /High Pass Filter) using windowing technique. i. Using rectangular window ii. Using hamming window iii. Using Kaiser window.

11. Design and verify Filter (IIR and FIR) frequency response by using Filter design and Analysis Tool.

12. Compute the Decimation and Interpolation for the given signal.

13. Real time implementation of an audio signal using a digital signal processor.

14. Compute the correlation coefficient for the two given audio signals of same length using a digital

MEVD-107 LAB II CMOS VLSI DESIGN

LIST OF EXPERIMENTS:

1. Design, simulate and implement an Adder (Min 8 Bit) using HDL by Xilinx FPGA
2. Design, simulate and implement a Multiplier (4 Bit Min) using HDL by Xilinx FPGA
3. Design, simulate and implement an ALU using HDL by Xilinx FPGA
4. Design, simulate and implement a Universal Shift Register using HDL by Xilinx FPGA
5. Design, simulate and implement Finite State Machine (Moore/Mealy) using HDL by Xilinx FPGA
6. Design schematic and simulate CMOS layout for half/full adder logic
7. Design schematic and simulate CMOS layout for flip flop Logic
8. Design schematic and simulate CMOS layout for synchronous counter logic
9. Design schematic and simulate CMOS layout for asynchronous counter logic
10. Design schematic and simulate CMOS layout for shift register logic
11. Design Schematic and simulate CMOS layout for FSM (Mealy/Moore) Logic
12. Design Schematic and simulate CMOS layout for Parallel Adder/Subtractor Logic